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ID: ABX00043

Date: 05/06/2024 Time: 12:38:09

File: TOP.SchDoc

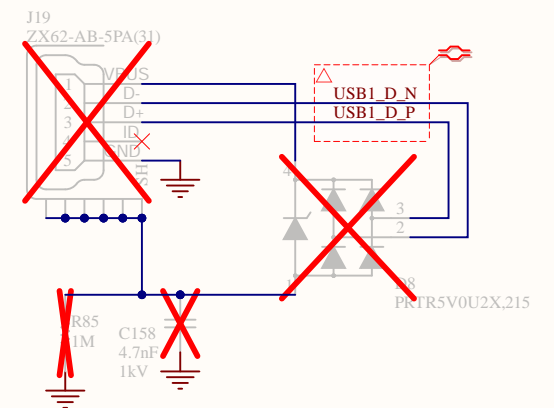
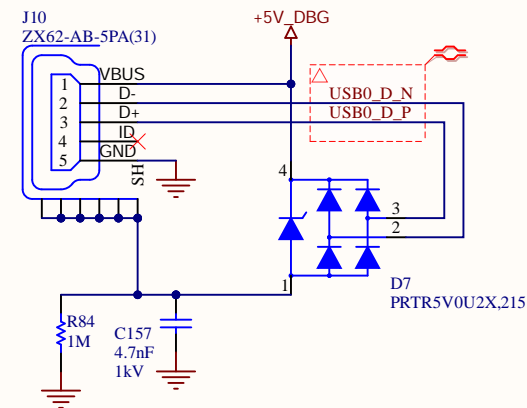
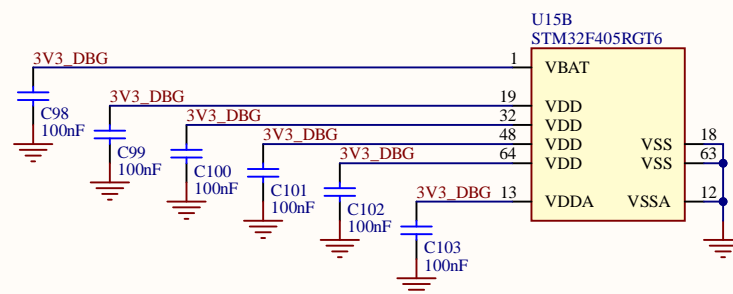
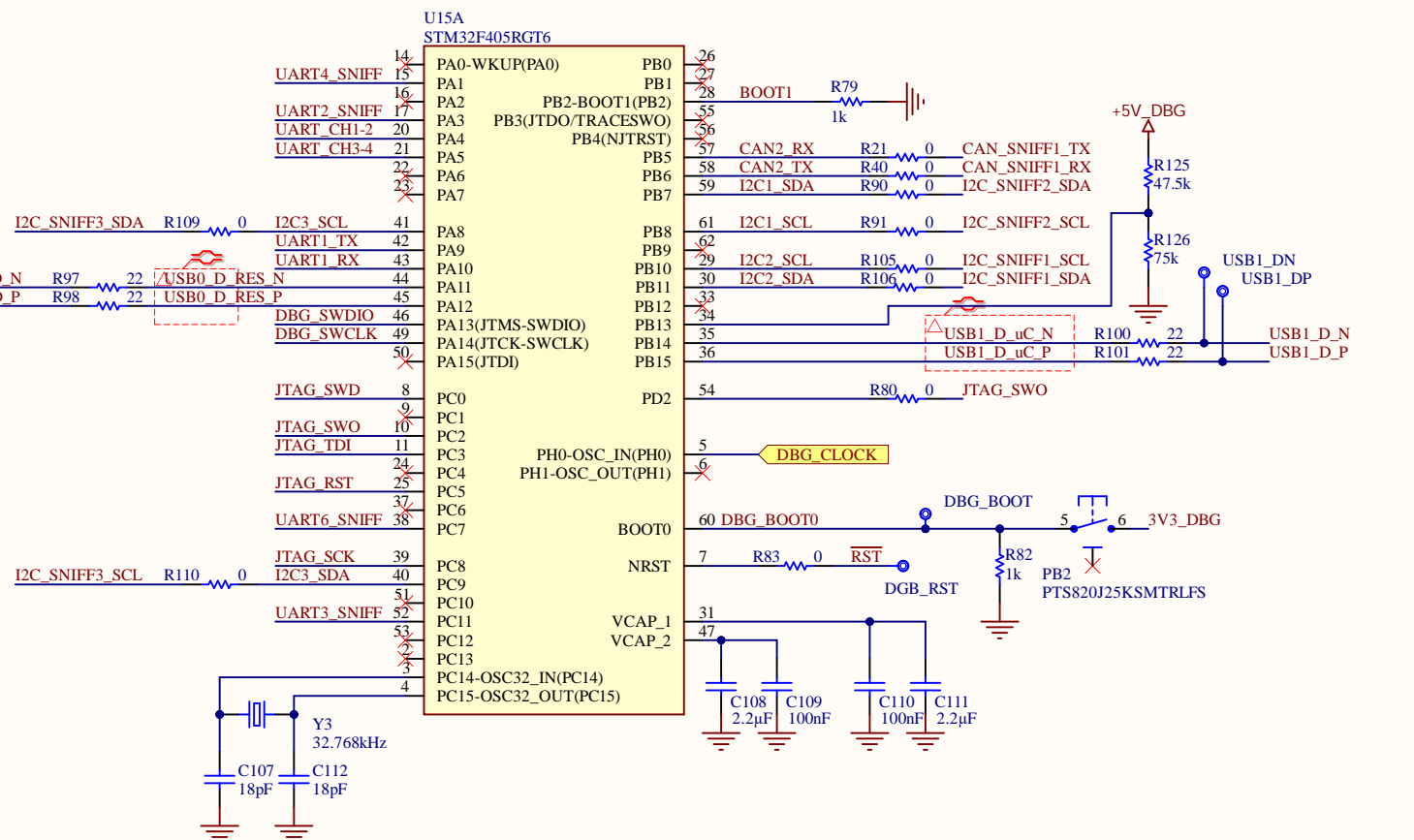
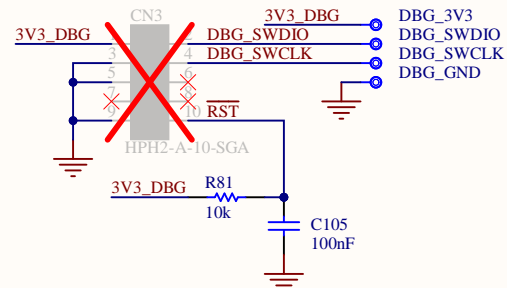
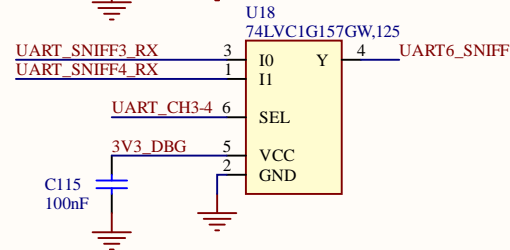
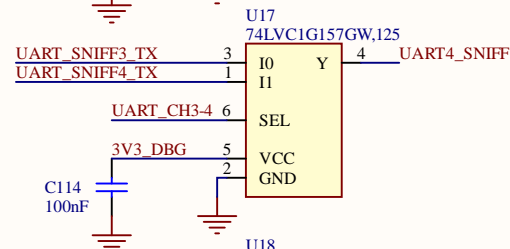
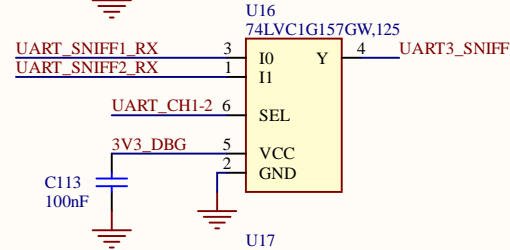
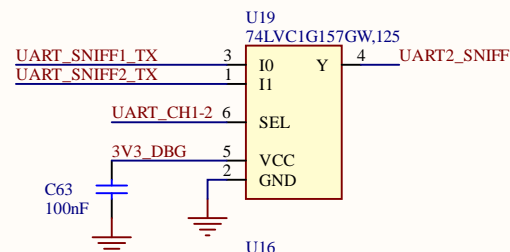
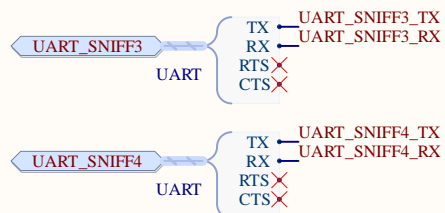
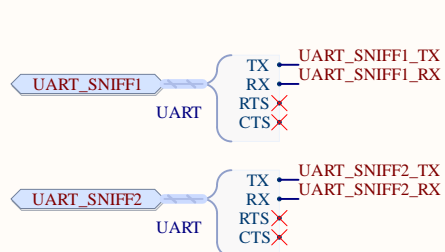
Revision: V3.12

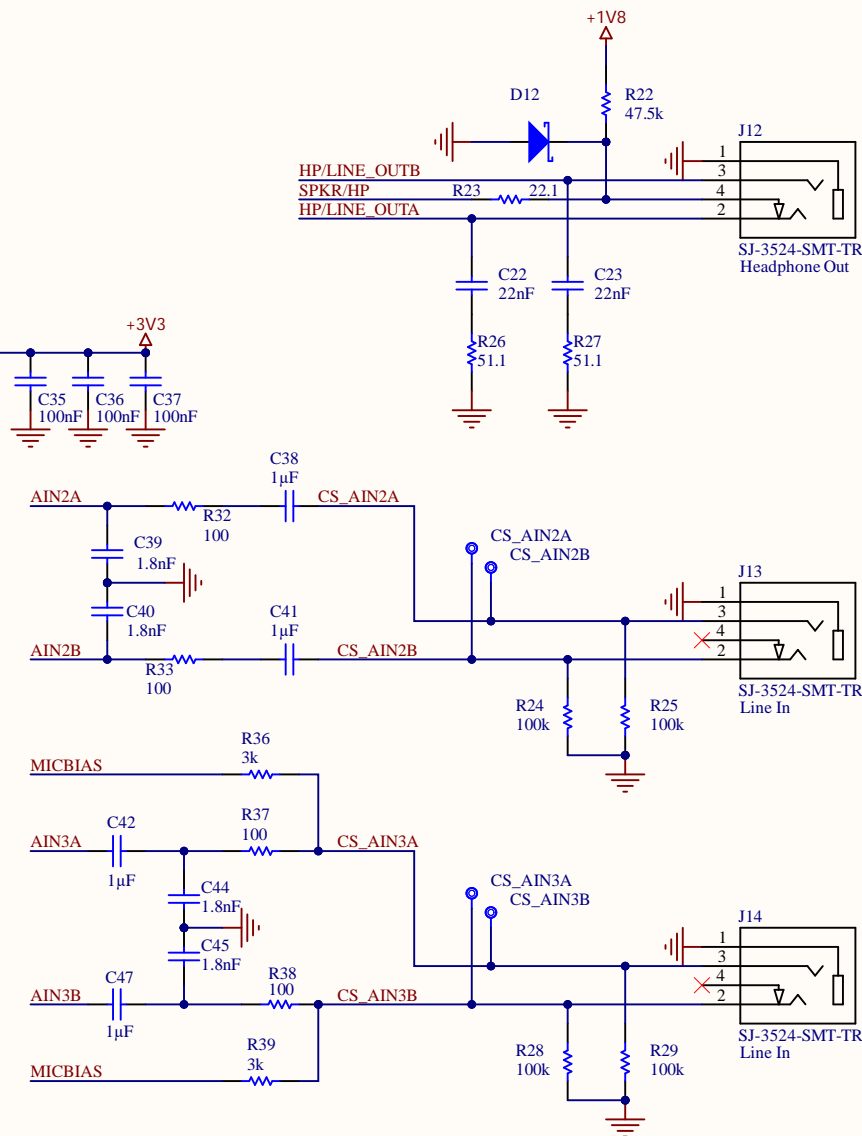
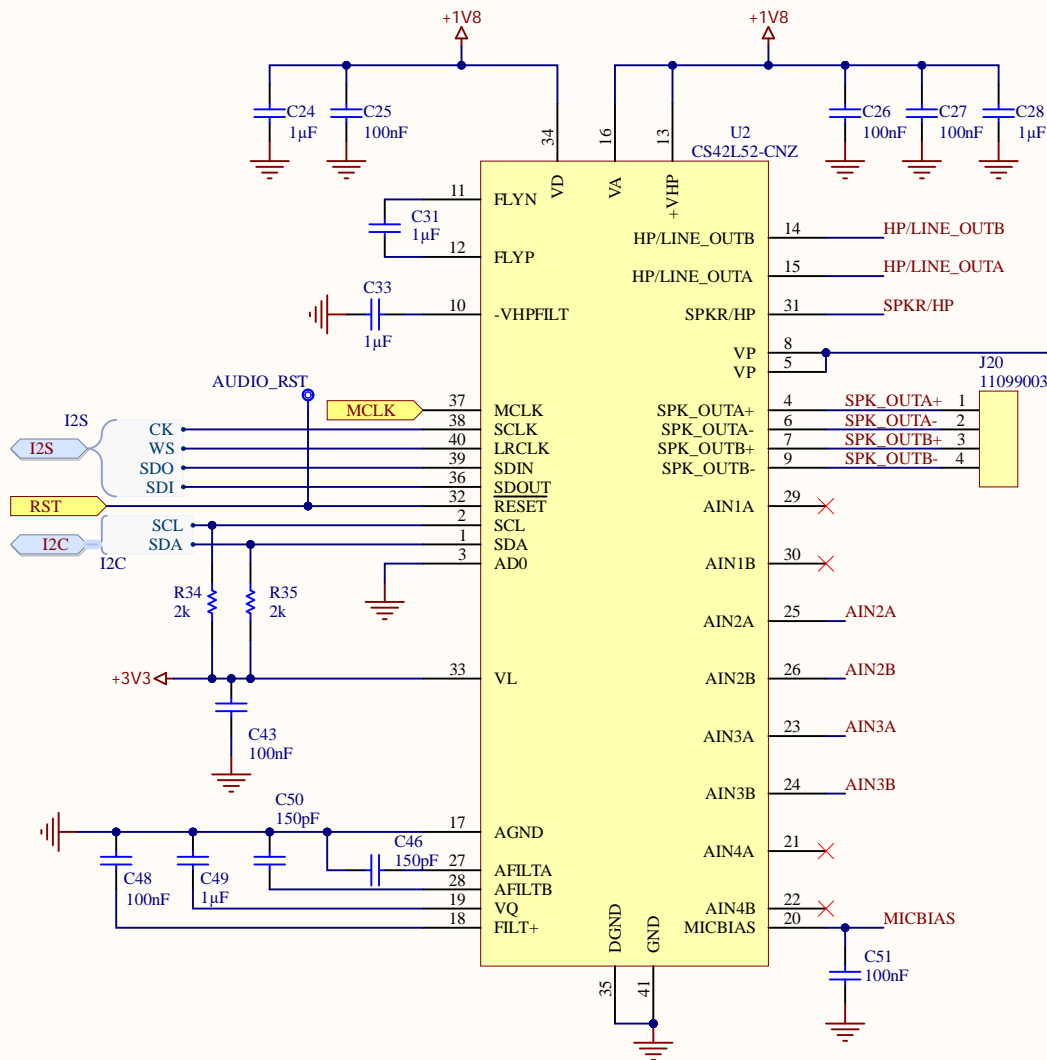
Sheet 1 of 14

Author: Arturo Guadalupi

RevAuthor: S. Navaretti







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Date: **05/06/2024**

File: **AUDIO.SchDoc**

Revision: **V3.12**

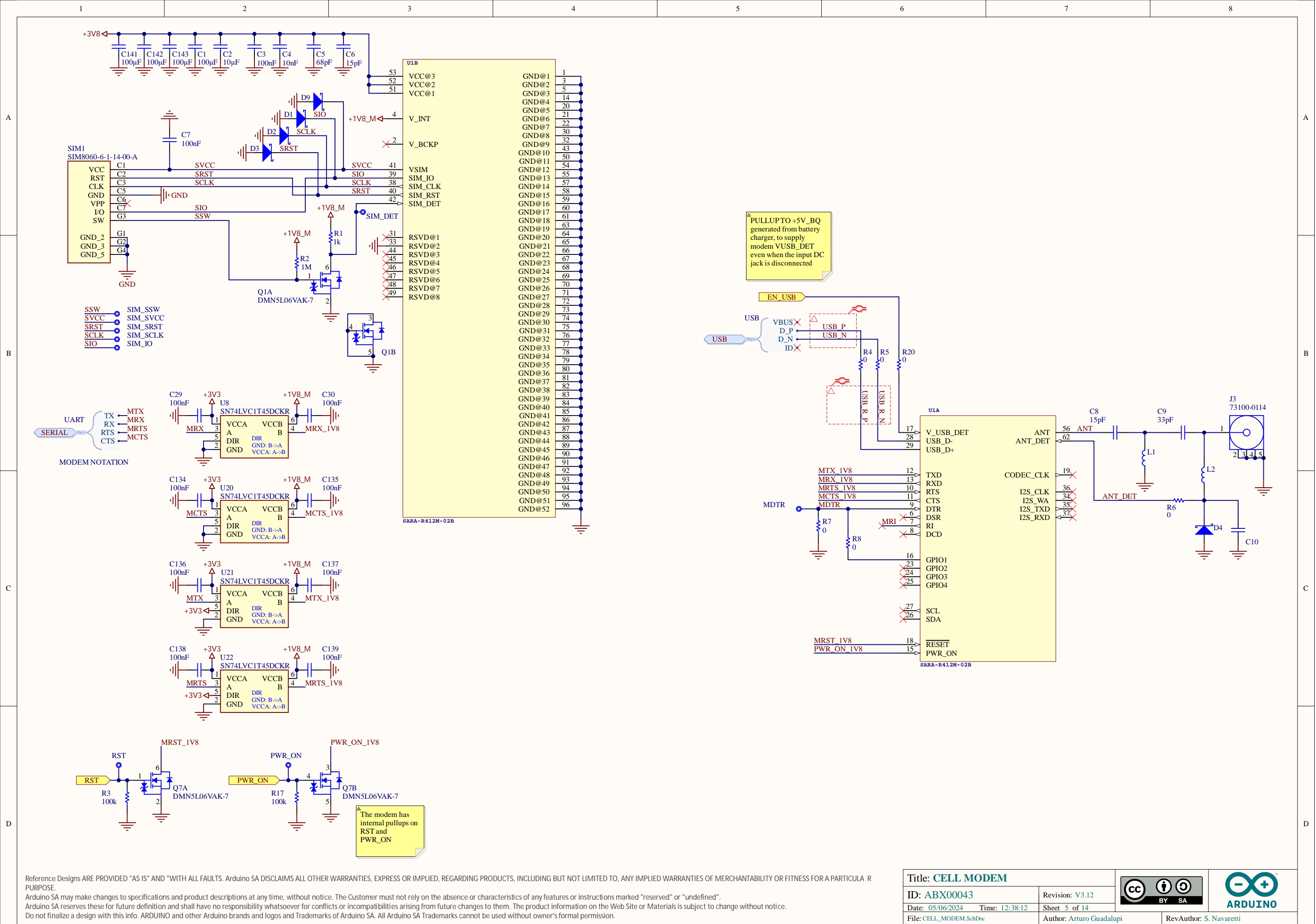
Time: **12:38:12**

Sheet **4** of **14**

Author: **Arturo Guadalupi**

RevAuthor: **S. Navaretti**





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Title: **CELL MODEM**

ID: **ABX00043**

Date: **05/06/2024** Time: **12:38:12**

File: **CELL_MODEM.SchDoc**

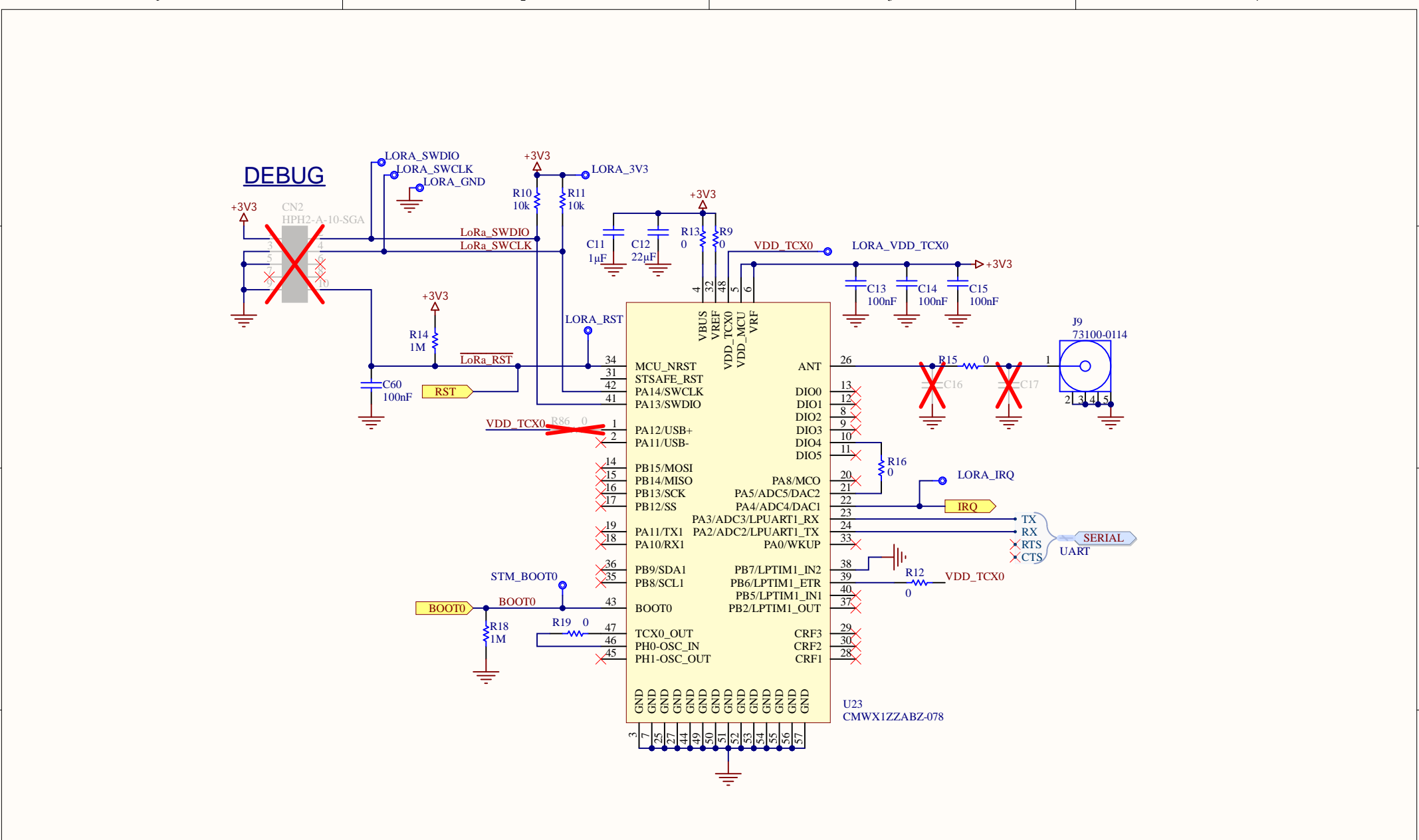
Revision: **V3.12**

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Author: **Arturo Guadalupi**

RevAuthor: **S. Navaretti**





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Title: **LORA**

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Revision: **V3.12**

Date: **05/06/2024** Time: **12:38:13**

Sheet **6** of **14**

File: **LORA.SchDoc**

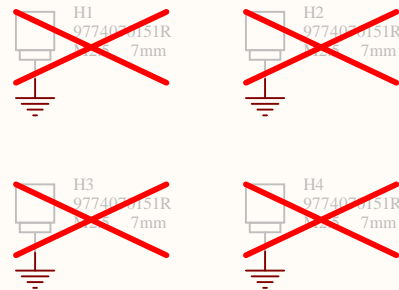
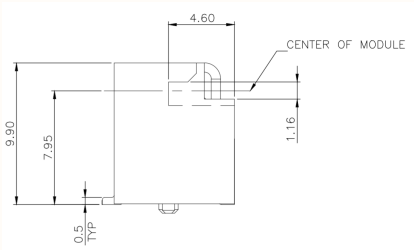
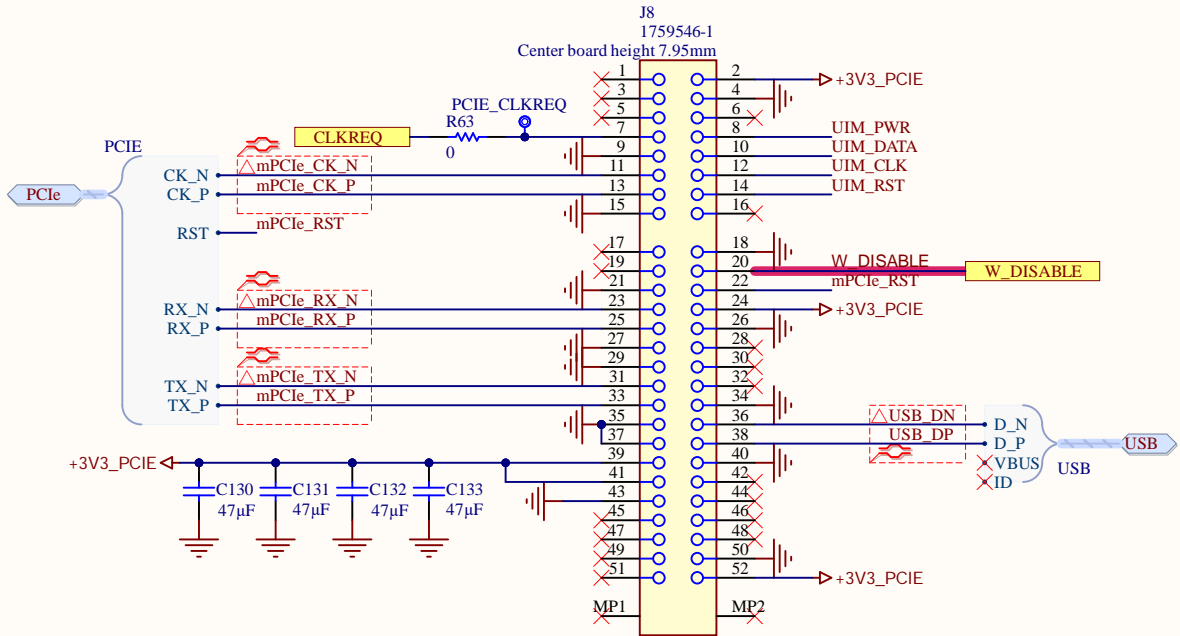
Author: **Arturo Guadalupi**

RevAuthor: **S. Navaretti**



Top side		Bottom side	
1		2	3.3V
3	Reserved****	4	GND
5	Reserved****	6	1.5V
7	CLKREQ#	8	VCC**
9	GND	10	I/O**
11	REFCLK-	12	CLK**
13	REFCLK+	14	RST**
15	N/C or GND	16	VPP**
Mechanical key			
17	Reserved	18	GND
19	Reserved	20	Reserved***
21	GND	22	PERST#
23	PERn0	24	+3.3Vaux
25	PERp0	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PETn0	32	SMB_DATA
33	PETp0	34	GND
35	GND	36	USB_D-
37	Reserved*	38	USB_D+
39	Reserved*	40	GND
41	Reserved*	42	LED_WWAN#
43	Reserved*	44	LED_WLAN#
45	Reserved*	46	LED_WPAN#
47	Reserved*	48	+1.5V
49	Reserved*	50	GND
51	Reserved*	52	+3.3V

*Reserved for future second PCI Express Lane (if needed). Pin 51 has changed to be W_DISABLE2#
**Reserved for future Subscriber Identity Module (SIM) interface (if needed)
***Reserved for future wireless disable signal (if needed)
****Reserved for future wireless coexistence control interface (if needed)



MPCI-L2 series

UIM_PWR 8
UIM_DATA 10
UIM_CLK 12
UIM_RESET 14

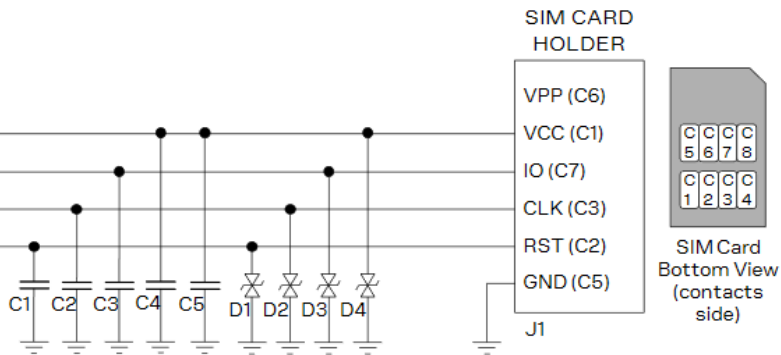
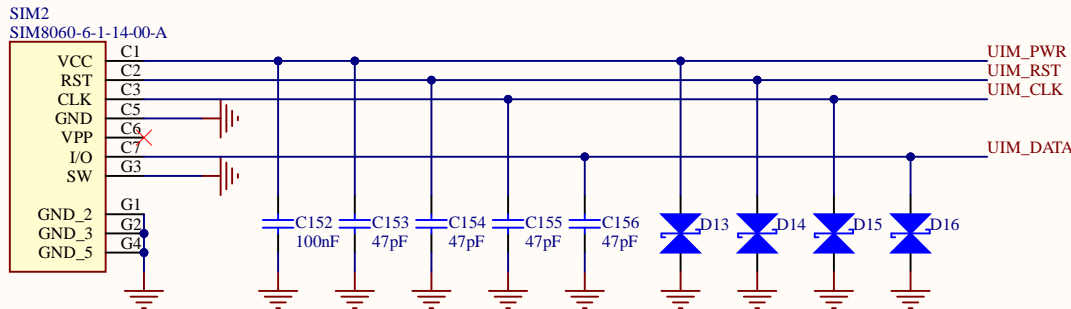


Figure 50: Application circuits for the connection to a single removable SIM card, with SIM detection not implemented



A

B

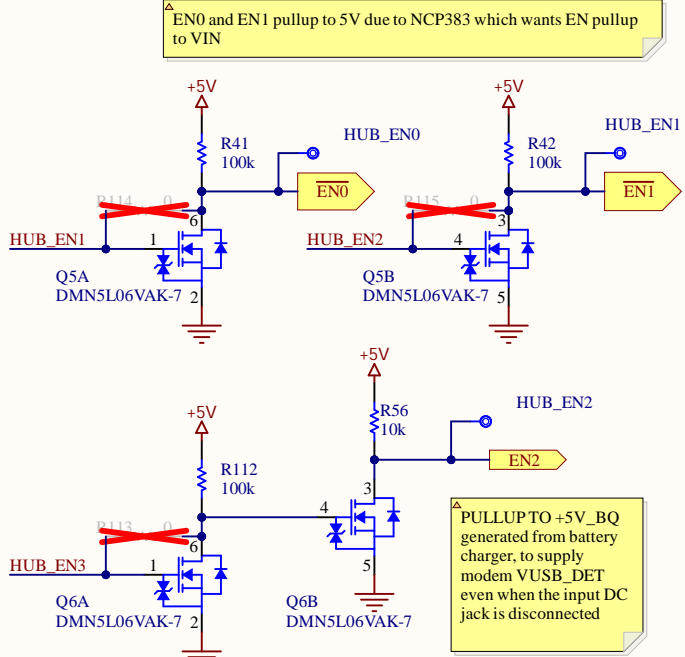
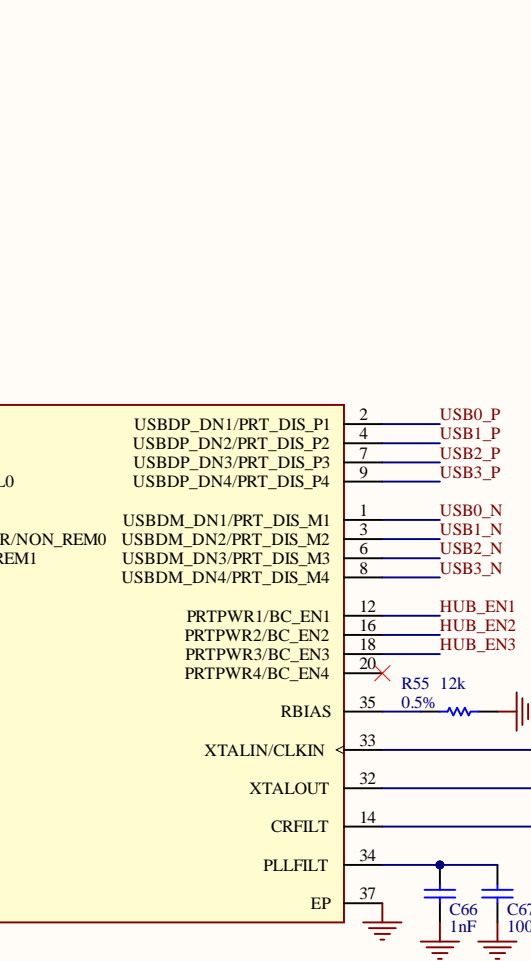
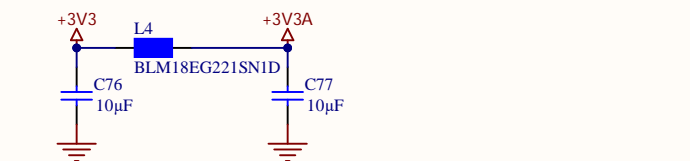
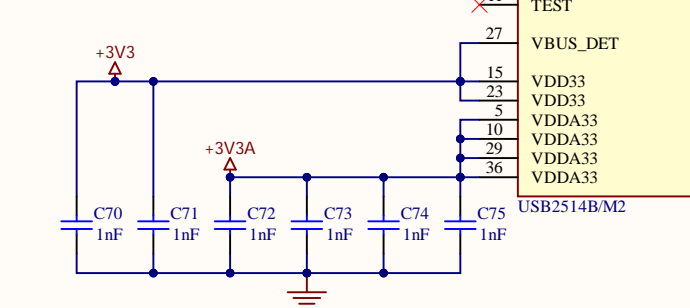
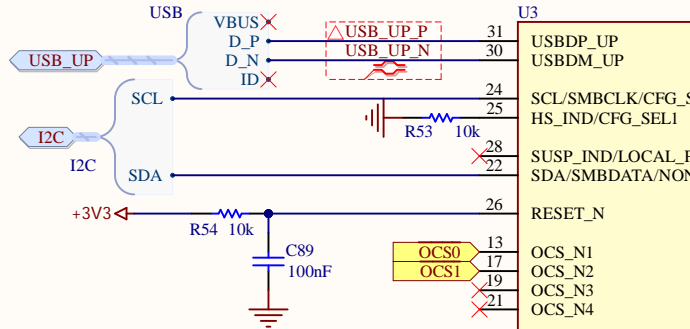
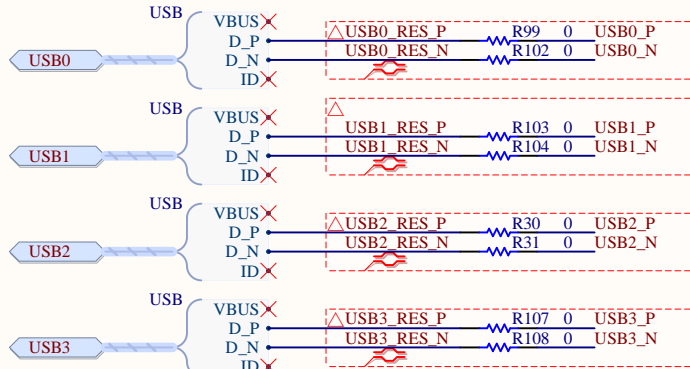
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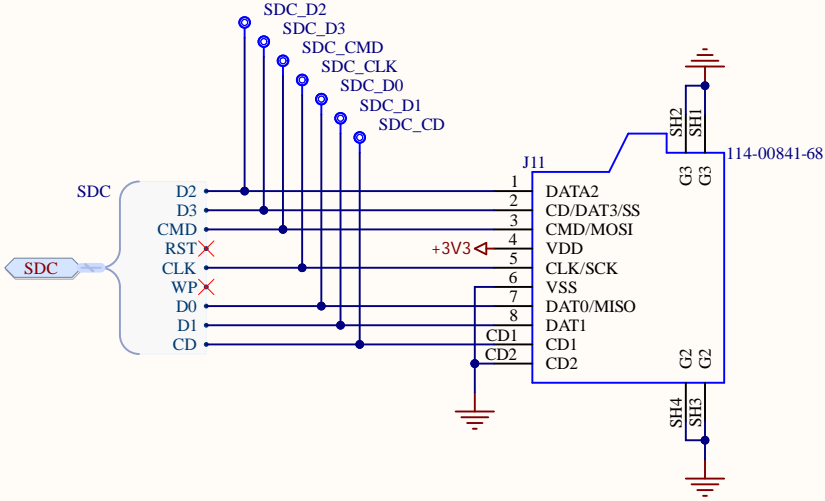
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Title: USB HUB		 	
ID: ABX00043			
Date: 05/06/2024	Time: 12:38:14	Revision: V3.12	Sheet 8 of 14
File: USB_HUB.SchDoc		Author: Arturo Guadalupi	RevAuthor: S. Navaretti



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Title: **SD CARD**

ID: **ABX00043**

Revision: **V3.12**

Date: **05/06/2024**

Time: **12:38:16**

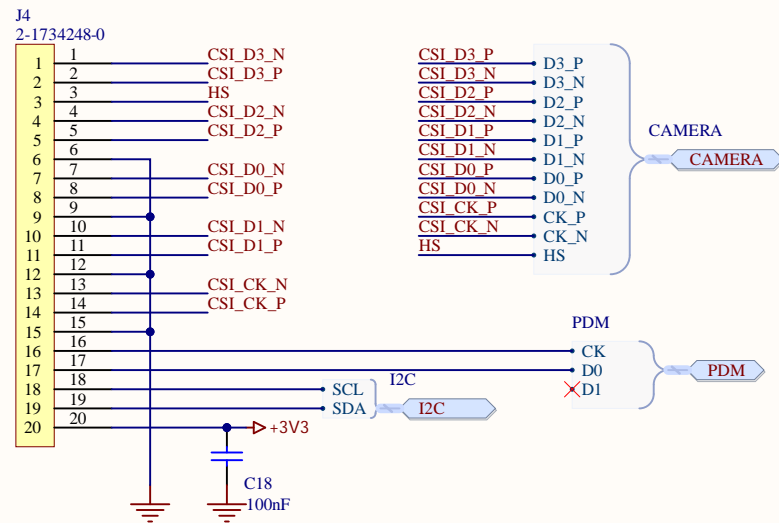
Sheet **10 of 14**

File: **SD_CONNECTOR.SchDoc**

Author: **Arturo Guadalupi**

RevAuthor: **S. Navaretti**







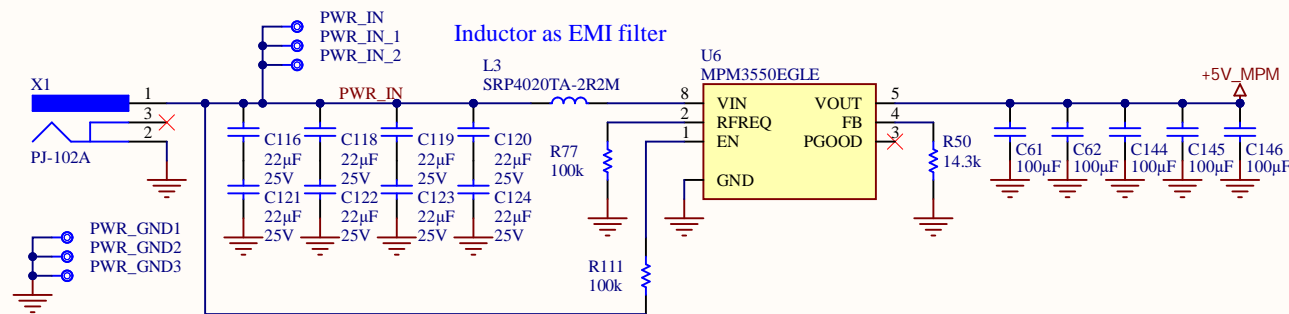
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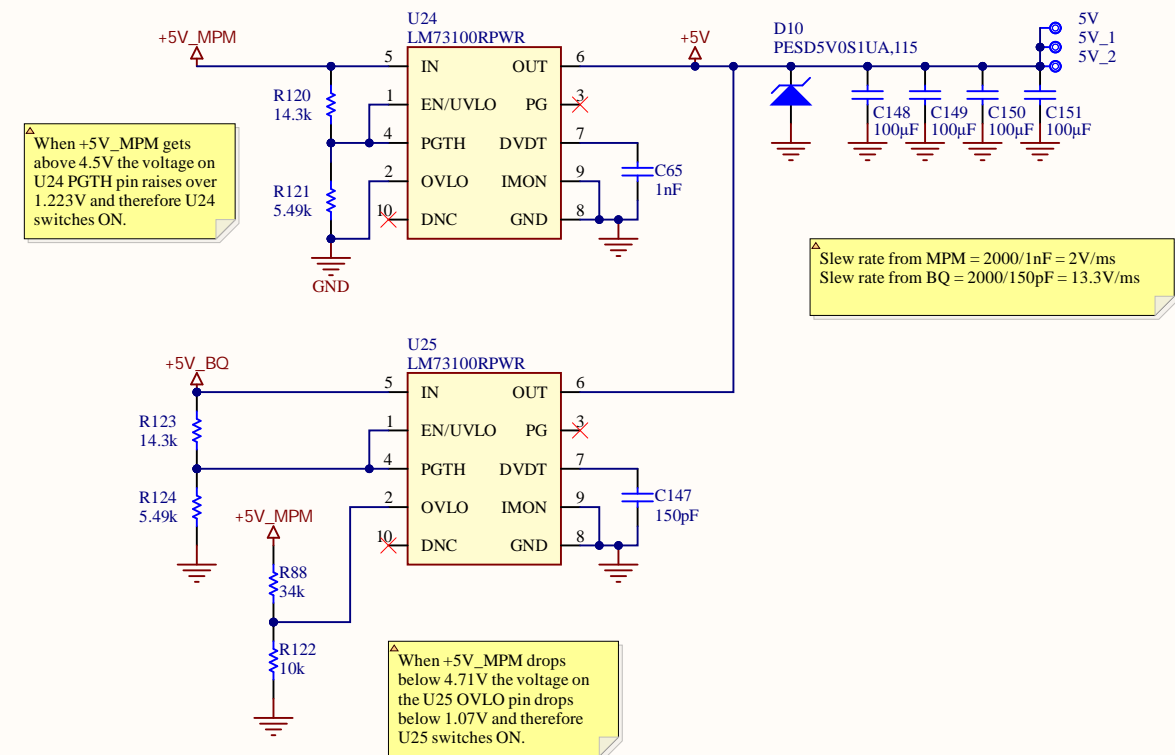
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Title: CAMERA CONNECTOR					
ID: ABX00043		Revision: V3.12			
Date: 05/06/2024	Time: 12:38:16	Sheet 11 of 14			
File: CAMERA_CONNECTOR.SchDoc		Author: Arturo Guadalupi		RevAuthor: S. Navaretti	

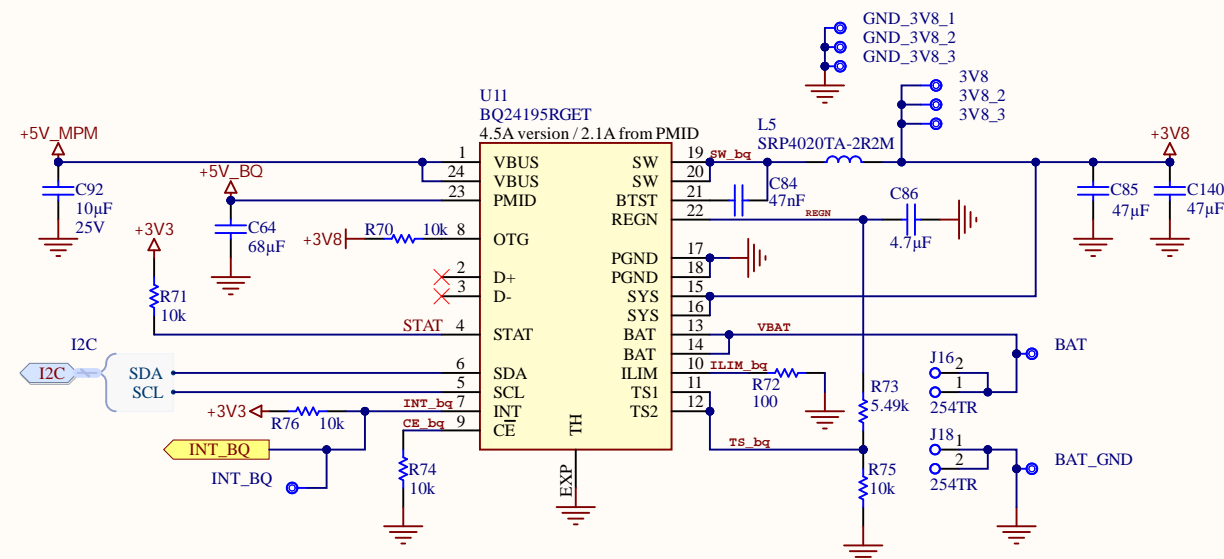
Power in from jack, +5V step down



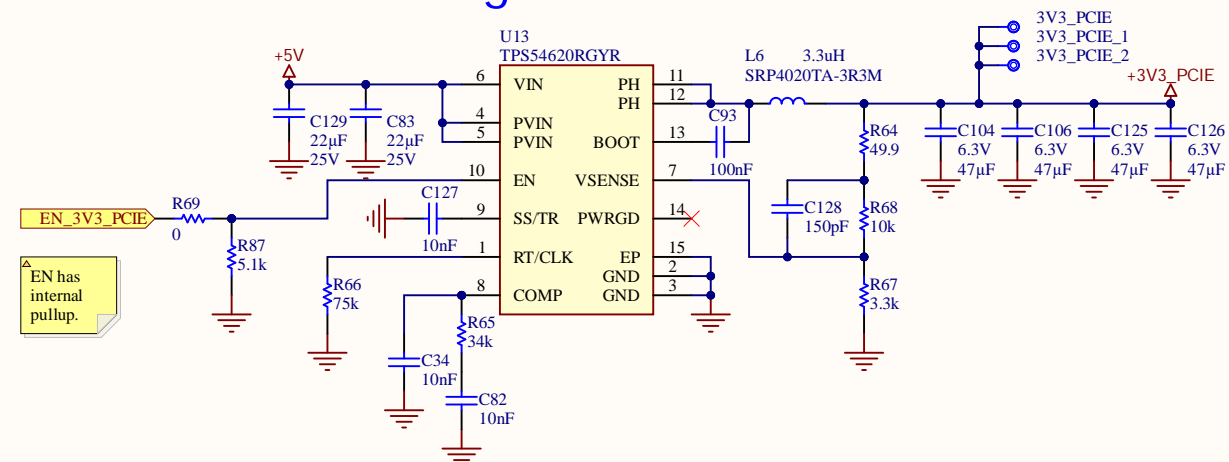
Power OR between +5V from jack or battery boost



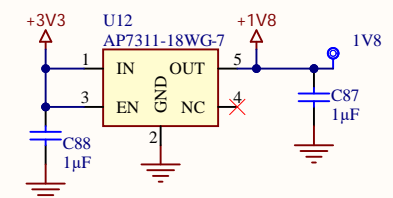
Battery charger and +5V boost from battery



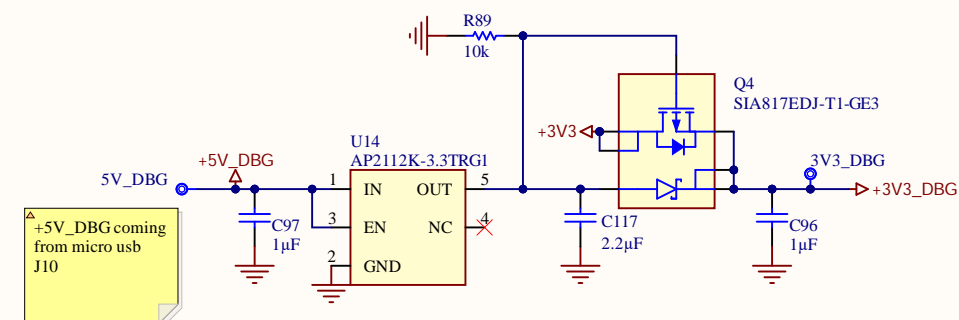
PCIE dedicated high current 3V3



Audio 1V8 linear regulator



Dedicated Debugger PWR



PIN DESCRIPTIONS

Pin	Name	RS-232	RS-485 Full Duplex	RS-485 Half Duplex
1				
2	GND		Ground	
3	T1OUT, B/Z	Transmitter 1 Output	Z Driver Neg Output	B/Z Neg Input/Output
4	T2OUT, A/Y	Transmitter 2 Output	Y Driver Pos Output	A/Y Pos Input/Output
5				
6	R1OUT	Receiver 1 Output	X	X
7	R2OUT, RO	Receiver 2 Output	Receiver TTL Output	Receiver TTL Output
8				
9				
10	SHDN		Low power shutdown mode when low	
11	SLEW		Data rate limited to 250Kbps when low	
12	FD_TX_TERM	X	120Ω Y-Z termination enabled when both TERM and FD_TX_TERM are high	X
13	TERM	X	120Ω A-B termination enabled when high	
14	RS-485/RS-232	0	1	1
15	HALF/FULL	X	0	1
16				
17	GND		Ground	
18	R2IN, A	Receiver 2 Input	A Pos Receiver Input	X
19	R1IN, B	Receiver 1 Input	B Neg Receiver Input	X
20	RE		Receiver enabled when low	
21	T2IN, DE	Transmitter 2 Input	Driver enabled when high	
22	T1IN, DI	Transmitter 1 Input	Driver TTL Input	
23				
24				
25	V-		Charge pump negative supply, 0.1μF from ground	
26	C2-		Charge pump cap 2 negative lead	
27	C2+		Charge pump cap 2 positive lead, 0.1μF	
28	V+		Charge pump positive supply, 0.1μF to ground	
29	C1+		Charge pump cap 1 positive lead, 0.1μF	
30	VL		Logic Supply for TTL Inputs and Outputs, V _L = +1.65V to +5.5V or tie to V _{CC}	
31	VCC		Main Supply, V _{CC} = +3.0V to +5.5V, bypass to ground with 1.0μF	
32	C1-		Charge pump cap 1 negative lead	

TABLE 3: RS-485/422 TX TRUTH TABLE

		INPUTS			OUTPUTS	
SHDN	RS-485/RS-232	DE/T2IN	DIT1IN	Z(B)/T1OUT	Y(A)/T2OUT	
0	X	X	X	1/8th unit load	1/8th unit load	
1	1	0	X	1/8th unit load	1/8th unit load	
1	1	1	0	1	0	
1	1	1	1	0	1	
X	0	X	X			RS-232 Mode

TABLE 4: RS-485/422 RX TRUTH TABLE

		INPUTS				OUTPUT
RS-485/RS-232	SHDN	HALF/FULL	RE	(A-B)	(Y-Z)	RO/R2OUT
1	0	X	X	X	X	High-Z
1	1	0	0	> -50mV	X	1
1	1	0	0	< -200mV	X	0
1	1	0	0	Floating	X	1
1	1	1	0	X	> -50mV	1
1	1	1	0	X	< -200mV	0
1	1	1	0	X	Floating	1
1	1	X	1	X		High-Z
0	X	X	X	X	X	RS-232 Mode

TABLE 5: RS-485/422 TERMINATION TRUTH TABLE

FD_TX_TERM	TERM	RS-485/RS-232	HALF/FULL	TX_TERM	RX_TERM
Pins 12-13	Pins 14	Pins 15	Pins 3-4	Pins 18-19	
X	0	1	0	-	-
0	1	1	0	-	ON
1	1	1	0	ON	ON
X	0	1	1	-	-
X	1	1	1	ON	-
X	X	0	X	-	-

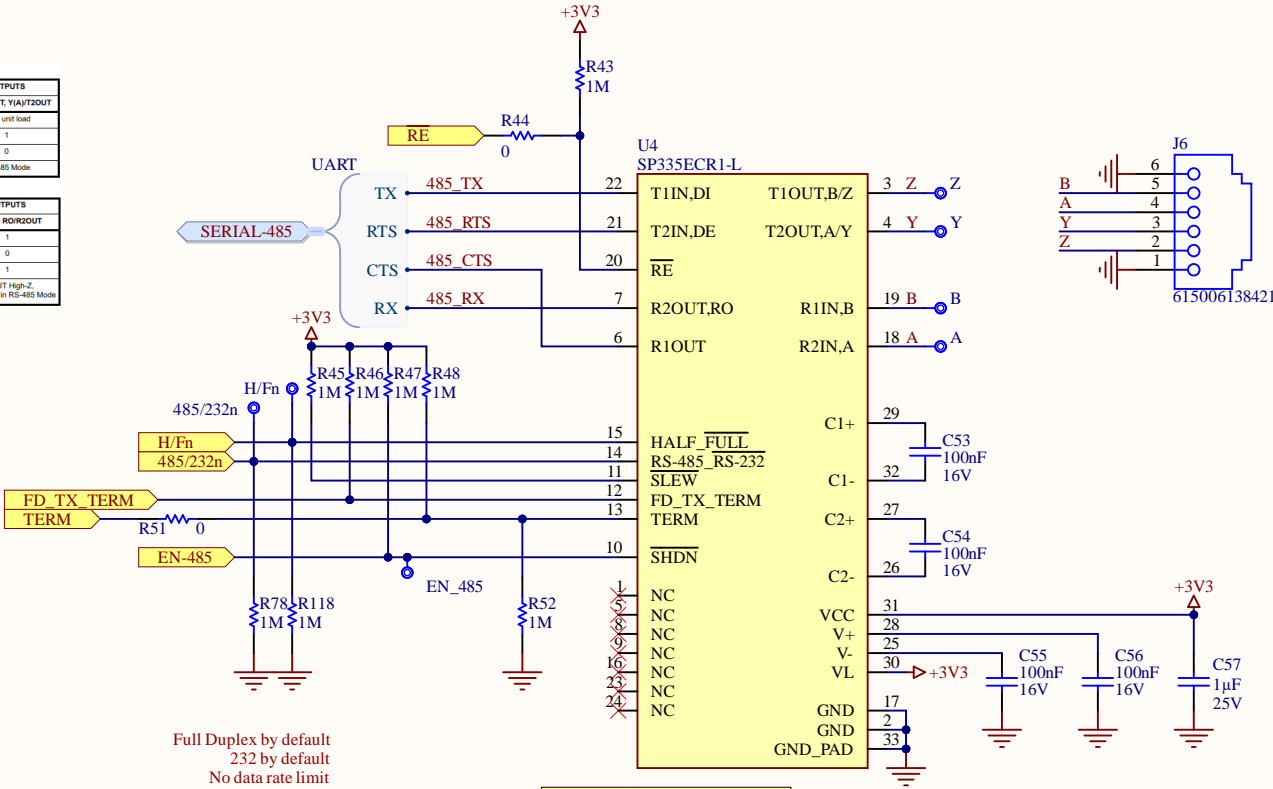
The DE and RE pins have no effect on the termination setting in any mode.

TABLE 1: RS-232 TX TRUTH TABLE

		INPUTS		OUTPUTS	
SHDN	RS-485/RS-232	DIT1IN, DE/T2IN	Z(B)/T1OUT, Y(A)/T2OUT		
0	X	X	1/8th unit load		
1	0	0	1		
1	0	1	0		
1	1	X	RS-485 Mode		

TABLE 2: RS-232 RX TRUTH TABLE

		INPUTS		OUTPUTS	
SHDN	RS-485/RS-232	B/R1IN, A/R2IN	R1OUT, RO/R2OUT		
X	0	0	1		
X	0	1	0		
X	0	Inputs open	1		
X	1	X	R1OUT High-Z, RO/R2OUT in RS-485 Mode		



Full Duplex by default
232 by default
No data rate limit
Enabled by default

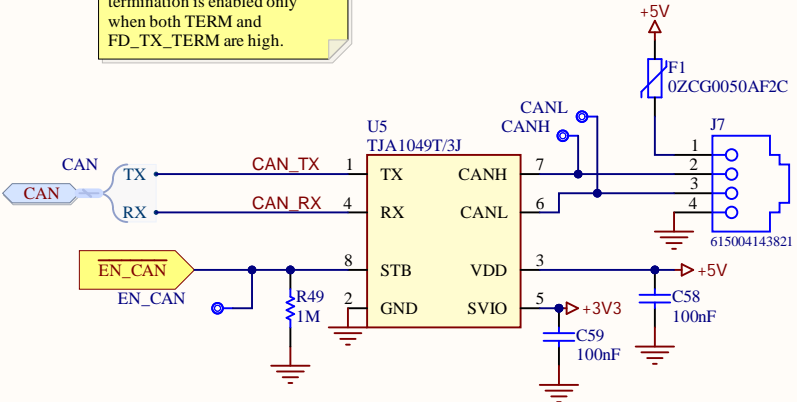
The full duplex driver termination is enabled only when both TERM and FD_TX_TERM are high.



RJ45 connector

RJ45 CAN Bus Pinout

RJ45 Pin #	RJ10 Pin #	Signal name	Signal Description
1	2	CAN_H	Dominant High
2	3	CAN_L	Dominant Low
3	4	CAN_GND	Ground
4	-	Reserved	Upgrade Path
5	-	Reserved	Upgrade Path
6	-	CAN_SHLD	CAN Shield, Optional
7	-	CAN_GND	Ground
8	1	CAN_V+	Power, Optional



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Title: **FIELD BUS**

ID: **ABX00043**

Date: **05/06/2024** Time: **12:38:18**

File: **FIELD BUS.SchDoc**

Revision: **V3.12**

Sheet **13** of **14**

Author: **Arturo Guadalupe**

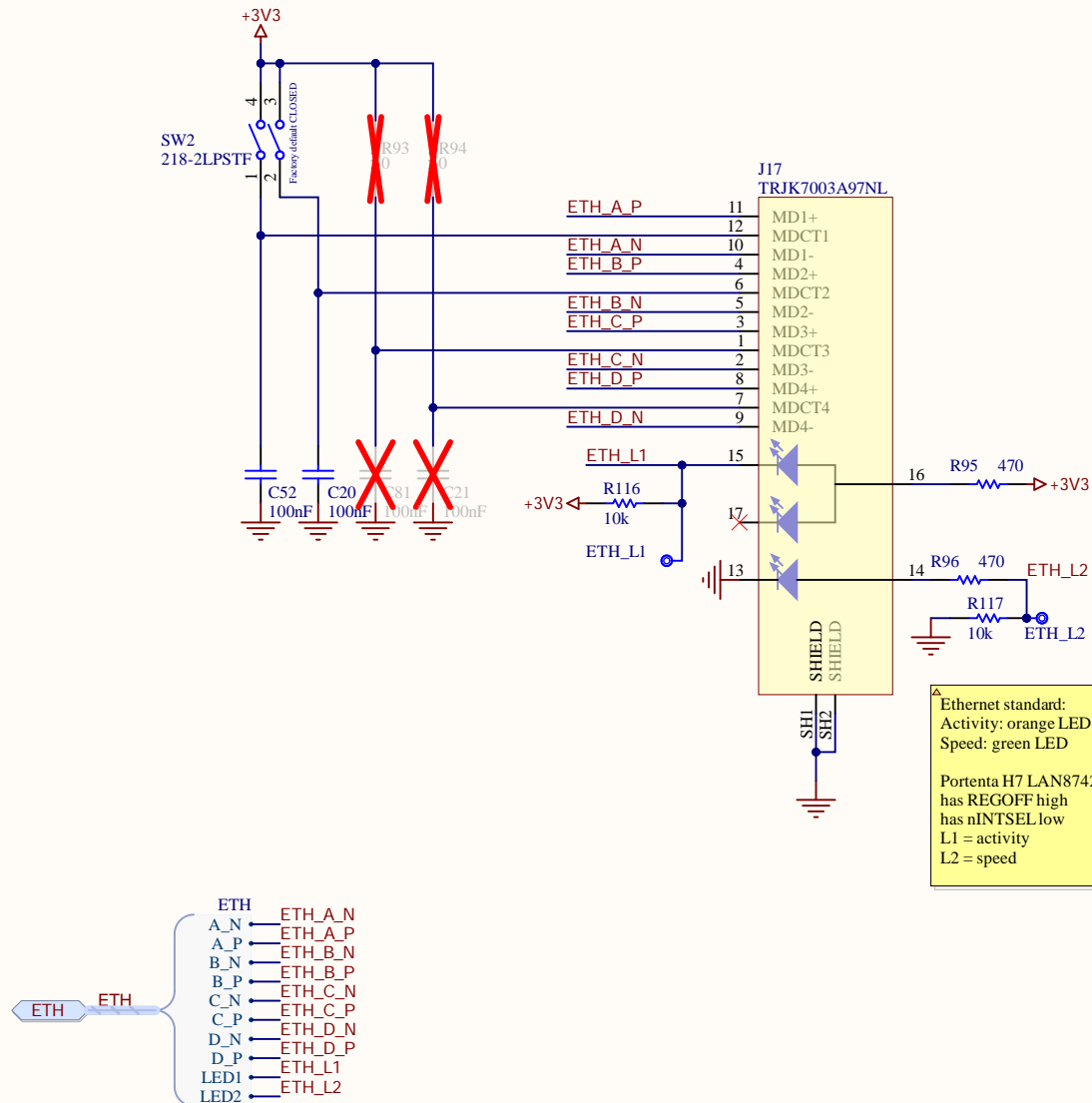
RevAuthor: **S. Navaretti**

A

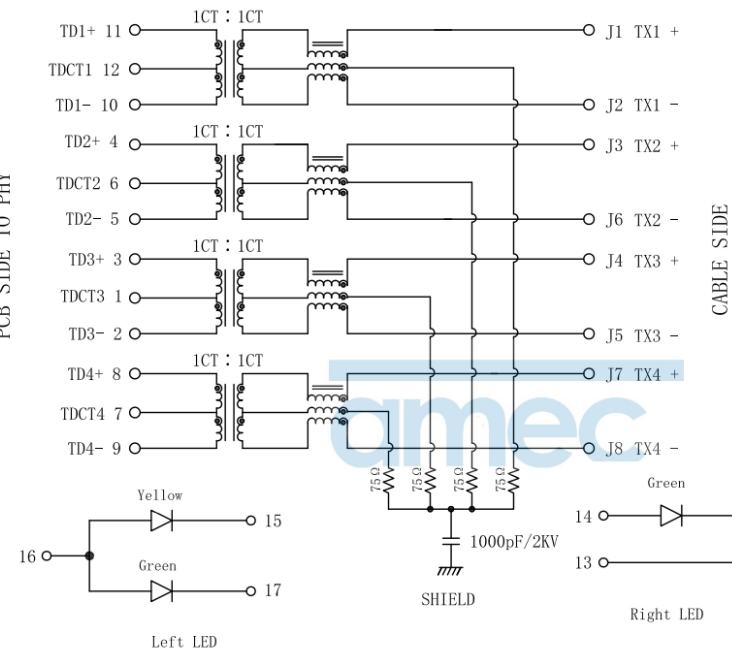
B

C

D



PCB SIDE TO PHY



A

B

C

D

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Title: **ETHERNET**ID: **ABX00043**Revision: **V3.12**Date: **05/06/2024** Time: **12:38:19**Sheet **14** of **14**File: **ETH_CONNECTOR.SchDoc**Author: **Arturo Guadalupi**RevAuthor: **S. Navaretti**